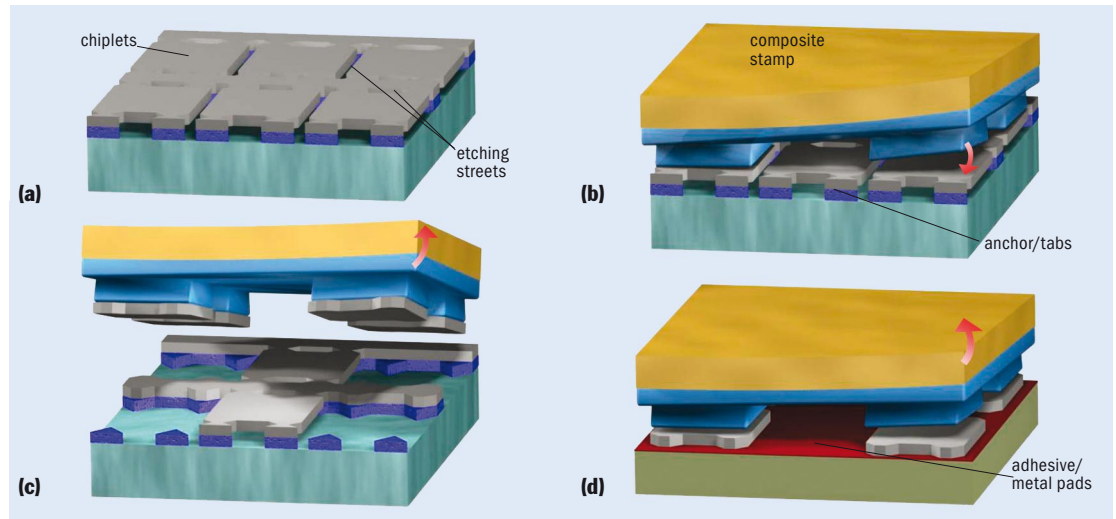


# Printing unites III-Vs and silicon

Semprius is refining and scaling a versatile printing process for uniting III-Vs with silicon. The technique will cut the cost of photovoltaics and RF and broadband sources, say **Kyle Benkendorfer**, **Etienne Menard** and **Joseph Carr**.



**Fig. 1.** The semiconductor printing process developed by John Rogers' team at the University of Illinois begins with the preparation of microstructures on conventional semiconductor wafers (a). A composite stamp is then laminated against this source (b), before it is quickly peeled away to leave the microstructures attached to the stamp (c). The stamp is then transferred to the target substrate and printed onto this platform, which can be coated with an adhesive layer (d).

A lot of time has been devoted to the tricky problem of combining the best attributes of compound semiconductors, like high mobility and a direct bandgap, with the low-cost, mature manufacturing processes of silicon CMOS. The efforts have brought success at the research level, but in many cases commercialization is still a distant dream.

One technique that does promise near-term commercialization, however, is a simple, scalable process for the heterogeneous integration of III-Vs and silicon. This process was invented at the University of Illinois, Urbana-Champaign, by John Rogers and his team. The technique, which can create unique architectures that will ultimately produce new high-performance, low-cost RF and broadband devices and high-spectral-response photovoltaics, is being licensed by us at Semprius, a spin-out based in Durham, NC (see box "The Semprius story so far" for more details about the company). We plan to refine this process for volume production and ultimately commercialize the technology over the next few years.

Our technology centers on a printing technique for transferring sub-millimeter sized, sub-micron thick "chiplets" – which could include individual compound semiconductor transistors or small circuits – from one substrate to another (see figure 1). With an elastomeric stamp, arrays of chiplets can be transferred from donor to acceptor substrates in a single process.

The process begins by bringing a stamp into intimate contact with chiplets formed at the surface of

compound semiconductor wafers (see figure 1 (b)). This stamp is then peeled back at a rate that removes the microstructures efficiently from the donor substrate, while maintaining their order and alignment (see figure 1 (c)). These chiplets are then printed onto the target substrate, which has been coated with an ultrathin film adhesive, and the stamp is peeled back ensuring full transfer of the microstructures.

Before this process can begin, the chiplet's dimensions are defined with a "delineation" process. This step involves using an etchant to produce streets around the chiplets and remove a release layer. The undercutting process can be applied to GaAs wafers with AlAs release layers and to GaN films grown on silicon (111) substrates – an orientation that is suitable for GaN growth, but not CMOS processing. When the underlying silicon is etched, "microbridges" are formed that hold the chiplets in place before they are transferred to CMOS-compatible silicon (100) (see figure 2 (b)).

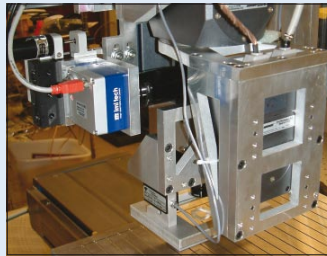
Our printing process has already printed single-crystal silicon, GaN and GaAs chiplets with thicknesses of 50 nm–100 μm and lateral dimensions ranging from 300 nm to a few millimeters. Examples include a 30 mm × 38 mm array of 24,000 silicon microstructures on a 100 mm GaAs wafer, which was produced with a process yield – including micromachining, pick up and release – of 95% (see figure 2 (c) and (d)). A reverse approach is possible, involving the printing of GaAs ribbons onto a silicon surface. We have successfully created many other structures with this approach, including silicon MOSFETs and

## The Semprius story so far

Semprius was founded in January 2005 with seed investment from Illinois Ventures. An additional \$4.1 million of series A funding was secured this April for product and business development from Illinois Ventures, Arch Venture Partners and Intersouth Partners.

The start-up currently employs five people, and expects its workforce to double by 2008. It is headed by CEO Joseph Carr, who has a strong pedigree in leading materials technology companies.

He was previously CEO of QD Vision and prior to that he worked



**Semprius** has built an automated printing tool for volume production.

for Osram Opto Semiconductors (OOS), where he held the roles of CEO of OSS Inc and general manager of the business unit for

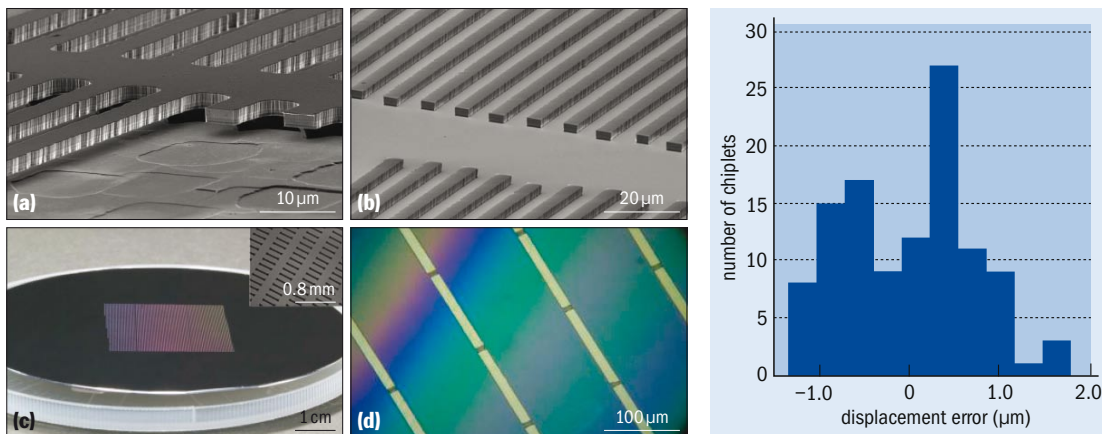
organic LED displays. He has over 20 years of experience working for the Dow Chemical Company.

Carr has also provided consultancy services to several start-ups and currently serves on the board of directors of several companies.

Another member of the Semprius team is Kyle Benkendorfer, senior director of business development, who has also been a consultant to several start-ups. Benkendorfer has over 23 years of experience in bringing early stage research to market

through his role as a technical and commercial manager at Dow Chemical. He has commercialized new semiconductor packaging materials in Japan, Korea, Taiwan, Singapore and the US; new polyurethane materials in Australia and New Zealand; spin-on dielectrics in North America and Europe; and light emitting polymers for use in organic LED displays in Japan and Taiwan.

A third key member of the Semprius' team is Etienne Menard, who is co-inventor of much of the company's technology



**Fig. 2.** (left) Printing can be used to transfer under-etched GaN ribbons from a Nitronex GaN-on-silicon (111) wafer **(a)** to a target silicon (100) wafer **(b)**. The microstructures are perfectly aligned after the wet release process, because their ends are tethered to the source wafer. The process can also produce a 30 mm × 38 mm array of 24,000 silicon microstructures on a 100 mm GaAs wafer **(c)**. GaAs ribbons printed on a glass substrate are shown in **(d)**. High-resolution scanning electron microscopy images suggests that fewer than 100 microstructures are missing from this array. **Fig. 3.** (right) Our prototype dry transfer printing tool fitted with a thin 24 mm × 24 mm composite transfer stamp produces deviations from perfect placement of typically only ±1 μm, which are caused by the tool and local distortions. This histogram was produced by processing 112 images captured with the tool's built-in CCD camera.

GaN MESFETs arrays, circuits featuring ring oscillators, differential amplifiers, logic gates, diodes and resistors – which have been interconnected to the underlying substrate using evaporated metal lines formed over the device's edge.

Our work has not been limited to the transfer of chiplets onto silicon and GaAs substrates: we have also developed this technique for transfer onto flexible plastics. On these platforms we have proven that printing does not dramatically alter device performance. Silicon chips on polyimide show mobilities of over 400 cm<sup>2</sup>/Vs and on/off ratios of over 10<sup>6</sup>, and GaAs transistors on polyethylene terephthalate produce typical I-V characteristics.

A key feature of our printing approach is the isolation of demanding fabrication processes to specific mother substrates. This means that different optimized and tailor-made processes can be applied to

the compound semiconductor chiplets and the receiving CMOS silicon wafer in the most efficient and affordable way. Complications from incompatible or inefficient processes are avoided.

The transfer printing step also delivers two major benefits: massively parallel transfer of chiplets and “geometric magnification.” Depending on the specific circuit configuration, each transfer step can print between hundreds and tens of thousands of chiplets simultaneously, which cuts costs and boosts manufacturing throughput. By designing the silicone stamp pad to pick up only one of every “n” chiplets, the printed substrate can also be populated over a larger area using a less dense array. On return to the source, the stamp can be indexed over one chiplet and the process repeated, thereby ensuring a very efficient use of the chiplets.

Another advantage of our process is that it can

## Rival approaches to integration

Many different commercial approaches have been developed to unite silicon and III-Vs.

The most straightforward option involves integrating various functions into sophisticated silicon or strained silicon chips, an approach referred to as "system-on-a-chip". This route benefits from standard manufacturing processes, but employs more complex designs to improve the circuit's performance. Companies can then use their existing manufacturing toolkit while dramatically increasing performance, but they have to accept a moderate rise in costs due to increased chip complexity.

Improvements in silicon technology are

increasing the popularity of this approach, but performance is still overshadowed by that of compound semiconductors.

An alternative and common approach involves the direct growth of III-Vs onto silicon. To ensure good-quality material, a lattice mismatch of less than 2% is required between the epitaxial film and the underlying substrate, which rules out the growth of GaAs-on-silicon.

Recently, several research groups have attempted to bridge or mute this mismatch by inserting a crystalline amorphous transition layer between the substrate and the device that has an intermediate lattice constant. Intel, Motorola and Philips have

all independently had success with this approach, but they say that commercial applications could be decades away.

The third popular route to heterogeneous integration is wafer-to-wafer or die-to-wafer bonding. Compound die or wafers are bonded to a silicon substrate processed with a receptor core, before the surplus base of the die or wafer is ground or etched away. This leaves the compound semiconductor circuitry intact within the silicon circuit.

This approach is used commercially, but suffers from the drawbacks of limited flexibility and high costs that are caused by significant material wastage during the process.

affordably handle and print chiplets with lateral dimensions of just 10  $\mu\text{m}$ , whereas traditional methods typically struggle to handle die with sides below 100  $\mu\text{m}$ . The etching step is also cheaper than dicing-based methods, which waste more material and produce less devices per wafer.

### Printing challenges

The primary challenge is to place the chiplets with enough accuracy. The elastomeric stamps used to do this are made by casting and curing a 1 cm thick piece of silicone rubber against a master substrate. They are capable of replicating the master's nanometer-scale patterns, so long as the stamp is made from a low-modulus silicone such as polydimethylsiloxane. However, single-layer stamps built with this soft material are prone to deformation during printing, which limits their use to coarse placement. Fortunately, this weakness can be addressed with advanced composite stamps that have low coefficients of thermal expansion, high in-plane mechanical rigidity and environmental stability, and a placement accuracy of less than  $\pm 2 \mu\text{m}$  (see figure 3).

The printing technique must also be compatible with the brittle chiplets. This brittleness stems from the fully fabricated chip's structure, which has several dielectric and metal layers on top of the thin epitaxial layer. These additional layers have a built-in strain that causes the ultrathin chiplets to bow after the wet-etching undercut process. However, this bowing can be avoided by optimizing the shape of the micro-bridge structures, so that they maintain the chiplet's flatness when they are attached to the wafer. Alternatively, the chiplet's mechanical stress can be offset with strain-balanced passivation layers.

Ours is not the only technique under commercial development for marrying silicon's cost and processing advantages with high-performance compound semiconductors. However, we believe that our approach has greater flexibility than alternative methods, which require improvements to silicon's performance, techniques to grow III-Vs directly

onto silicon and wafer-to-wafer technologies (see box "Rival approaches to integration").

One market that could benefit from our approach to circuit production is GaAs power-module manufacture. Discussions with several component makers and cost models produced by an industry expert have revealed that our printing approach could lead to cost savings through more effective use of GaAs and silicon. These savings result from using GaAs to make the transistors and the silicon CMOS substrate to form other components in the circuit, such as resistors and capacitors. This cuts the compound semiconductor real estate for each power-amplifier module and enables the costs of these units to approach CMOS silicon levels.

We are also targeting high-efficiency, high-spectral-response photovoltaics. Printing techniques can cut the production costs for these devices because an optimized combination of different materials can be brought together that offers high performance at low cost. Our process also offers further savings through wafer reprocessing, because our street etch process only removes a few microns of material.

We are now working to scale up a robust printing process to address both of these markets, and also markets involving active matrix display backplanes, large-area sensor arrays, such as X-ray detectors, and flexible electronics, such as smart packaging and RFID tags. We are also developing partnerships with companies that are expert in certain target markets and we are keen to engage more partners. We expect that our technology will be commercialized in the next few years. ●

### Further reading

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### About the authors

**Joseph Carr** is Semprius' CEO (right), **Kyle**

**Benkendorfer** (kyle. benkendorfer@semprius.com)

is the company's senior director of business development (left), and

**Etienne Menard** (middle) is a founding scientist at Semprius who co-invented a large proportion of the company's technology. The authors thank all the researchers in John Rogers group who prepared the GaAs and GaN heterogeneously integrated substrates.